Single Event Effects (SEE)  
Mechanism and Effects  

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Based on RADECS Short Course 2003 by S.Duzellier
Outline

• Introduction
• Basic Mechanism
• Overview on Non-Destructive Effects
• Overview on Destructive Effects
• Conclusion
Introduction

• SEE is electrical noise induced by the natural space environment (high energy ionising particles)
  – Ionisation mechanism

• Results in data corruption, transient disturbance, high current conditions (non-destructive and destructive effects)

• Affects many types of devices and technologies

• SEE can if not handled well cause unwanted functional interrupts or in worst case catastrophic failures.
Introduction

- Energetic Particles Causing Single Event Effects
  - Galactic cosmic rays
  - Cosmic solar particles (heavily influenced by solar flares)
  - Trapped protons in radiation belts
Outline

- Introduction
- Basic Mechanism
- Overview on Non-Destructive Effects
- Overview on Destructive Effects
- Conclusion
Mechanism for Single Event Effects

Each particle produces an ionization track

Most protons pass through the device with little effect

A few protons cause nuclear reactions

Short-range recoil produces ionization

a) Heavy ions (ionization by each particle)

b) Protons (nuclear reaction needed to produce recoil)

What about e.g. trapped Electrons?

After: A. Johnston, JPL

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EPFL Space Center 9th June 2009
Mechanism for Single Event Effects

- Charge Collection
  - Prompt component:
    - drift / funneling
      (high field regions)
  - Delayed component:
    - diffusion
      (low field regions)

After: I. Nashiyama, IEEE TNS, VOL. 40-6, 1993
Mechanism for Single Event Effects

- Charge collections generated in pn-junction typically leads to a shunt effect or bipolar amplification
  - Circuit design and technology dependent

After: I. Nashiyama, IEEE TNS, VOL. 40-6, 1993

After: A. Johnston, JPL
Summary Basic Mechanism

Ionisation from an ion trajectory

Charge Collection Mechanism in pn-junctions

The device type and technology and the localisation and amount of injected charge will define if a SEE will be triggered and the type of the SEE.
**Sensitive Volume SV**

The volume responsible for charge collection for a SEE

– \( \mu \text{m}^3 \)
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SEE Cross Section Curve vs LET

- Cross section (CS or $\sigma$) for a SEE measures the probability for a SEE to occur
- The Cross Section is a function of LET
- Below LETth the collected charge in the SV is too low to induce the SEE
- Saturation cross section ($CS_{sat}$ or $\sigma_{sat}$) defines the upper limit for SEE.
  - An ion injecting more charge in SV will not increase SEE probability

LET threshold (LETth) and Saturation Cross Section ($\sigma_{sat}$) is key measures of Single Event Effects (SEE)
Terms and Units

- **Linear Energy Transfer function** \( \text{LET} \) (or Stopping Power)
  - \( \text{MeV-cm}^2/\text{mg} \)

- LET threshold \( \text{LET}_{\text{th}} \)
  - \( \text{MeV-cm}^2/\text{mg} \)

- Critical Charge \( Q_C \)
  - \( \text{pC} \)

- Cross section \( \text{CS} \) (or \( \sigma \))
  - \( \text{cm}^2 \) or \( \mu\text{m}^2 \)

- Saturation Cross section \( \text{CS}_{\text{sat}} \) (or \( \sigma_{\text{sat}} \))
  - \( \text{cm}^2 \) or \( \mu\text{m}^2 \)

- Sensitive Volume \( SV \)
  - \( \mu\text{m}^3 \)
Overview on Non-Destructive Single Event Effects

• Events which momentary or permanently change state of a device or cell/node without not affecting the functionality.

• Main types
  – Single Event Upsets SEU
  – Single Event Functional Interrupts SEFI
  – Single Event Transients SET
Single Event Upsets SEU

– Change of state in storage element
  • Memory cell
  • Registers
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**Single Event Upsets SEU**

When SEU current $I_{SEU}$ exceeds restoring current from cross-coupled inverter such that the node voltage drops below $V_D/2$ for too long, an upset occurs.

(After Baumann)
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**Single Event Functional Interrupts SEFI**

- Event leading to temporal loss of device functionality
  - Recovered by reset or power cycle
  - Often induced from SEU in Control Registers
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**Single Event Functional Interrupts (SEFI)**

- **Advanced Memories**
  - Internal test modes
  - Microprogrammed cell architecture
- **Flash Memories**
  - Dominant effect
  - “Crashes” internal state controller and buffers
- **Xilinx Programmable Logic Arrays**
- **Microprocessors**
  - Many categories of responses
  - Detection and recovery are very difficult problems

*After: JPL course by G. Swift*
**Single Event Transients SET**

- Transients on external signals e.g. comparators
- Internal transients in e.g. CMOS leading to erroneous data
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**Single Event Transients (SET)**

Ion strike in e.g. a comparator

May affect subsequent circuits if not well filtered in design

- Heavy Ions
  - LET = 7.3 MeV·cm²/mg
  - $\Delta V_{\text{in}} = 25$ mV
  - Load Resistor = 1.5 k

After: JPL course by G. Swift
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**Single Event Transients**

Strongly depend on bias condition

Cross section curves for transients in a comparator

![Graph showing cross section curves for transients in a comparator](image)

- **Component Tests**
  - $\Delta V_{OUT} = \{-0.5 \text{ V}, -1 \text{ V}, -1.5 \text{ V}, -2 \text{ V}\}$

- **Circuit Module Tests**
  - $(\Delta V_{OUT} \approx 3 \text{ V})$

- $V_{CC} = 5 \text{ V}$
- Load resistance = 5.1 K
- $\Delta V_{IN} = 2.5 \text{ V}$

*After: JPL course by G. Swift*
Overview on Destructive Single Event Effects

• Events which interrupt device function and permanently damage the device without external interaction

• Four main types
  – Single Event Latch-up SEL
  – Single Event Burnout SEB
  – Single Event Gate Rupture SEGR
  – Single Event Hard Errors SHE
Single Event Latch-up SEL

Latchup can cause circuit lockup and/or catastrophic device failure

- If an energetic particle produces $I>I_L$, $\beta_n\beta_p>1$ and $V_{DD}>V_H$, then latchup will occur
- As technology scales, soon $V_{DD}<V_H$ and latchup is no longer a problem
- Epi reduces $R_n \Rightarrow$ increase latchup threshold
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**Single Event Latch-up SEL Facts**

- Triggered by heavy ions, protons, neutrons
- May be catastrophic
- Only recovered by power cycle
- SEL is strongly temperature dependent
  - Threshold for latchup decreases at high temperature
  - Cross section increases as well
- Modern devices may have many different latchup paths
  - Both high current and low current SELs can occur
  - Characterization of latchup is a difficult problem for complex circuits

*SEL is a critical effect with potential catastrophic impact on space craft systems*
  - SEL sensitive components shall as far as possible be avoided
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Single Event Latch-up SEL Temperature Dependence

Temperature Dependence of Basic Parameters

- $V_{BE}$ drops from 0.7 to 0.5V at 125 °C
- Well resistance doubles at 125 °C compared to room temperature

Saturation cross section increases with temperature

Threshold LET decreases with temperature

After: JPL course by L. Scheick
Single Event Latch-up SEL Counter Measures

• SEL Detection and Mitigation
  – Current limiting devices can’t stop latch-ups or low current latch-ups
  – Detection circuits can’t stop all latch-ups
    • Some devices have latch-up modes which are always destructive
  – Mitigation may not be fast enough
  – Thorough testing required to ensure that all latch-up events are detected
Single Event Latch-up SEL Technology Options

- **Device type**
  - Bulk CMOS latches worst
    - Commercial off-the-shelf devices (COTS)
  - CMOS deposited on epitaxial layer may improve SEL immunity
    - Some COTS - More Expensive
    - Not always effective (e.g., K-5 processor)
  - SOI and isolated oxides are mostly immune
    - Very expensive
    - Limited availability
Single Event Hard Errors SHE

- Large rare energy depositions can cause individual cells to be unable to change state
  - Referred to as a “stuck bit” in memory
    - This is believed to be a micro-dose effect
  - Micro latch-ups can cause a fraction of bits to be unable to change state
    - Power cycling is required
Single Event Burnout SEB

- **Mechanism:**
  - Localized current in body of device turns on parasitic bipolar transistor
    - Creating direct current path between drain and source
  - Roughly analogous to second breakdown in power transistors
  - Devices with low doping concentrations are most susceptible

- Triggered by heavy ions, and possibly by protons and neutrons

- Always destructive

- CMOS, power BJTs and FETs and MOSFETs can be susceptible
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**Single Event Gate Rupture SEGR**

- Triggered by heavy ions
- Always destructive to device
- Dependent on angle of incidence
- Dependent on electric field in gate oxide
  - May also occur with zero electric field over gate oxide
  - Interplay between pulsed current in drain region and oxide field
- Synergy between TID and SEE
- Power MOSFETs most susceptible
  - Some modern programmable devices are also susceptible
## Single Event Effects - Summary

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<th>Description</th>
<th>Examples</th>
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<td>Memories, latches in logic devices</td>
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<td>Single Event Functional Interrupt (SEFI)</td>
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<td>Single Hard Error (SHE)</td>
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<td>Single Event Transient (SET)</td>
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<td>Single Event Latchup (SEL)</td>
<td>High-current conditions</td>
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<td>Single Event Snapback (SESB)</td>
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<td>Rupture of gate dielectric due to high electrical field conditions</td>
<td>Power MOSFETs, Non-volatile NMOS structures, VLSIs, linear devices …</td>
</tr>
</tbody>
</table>

Non Exhaustive, more in ECSS E-ST-10-12C
Conclusion

• SEE is a disturbance in EEE components induced from high energetic particle by ionisation
  – Protons
    • indirect ionisation (mostly)
  – Heavy ions
    • direct ionisation

• SEE can be
  – Destructive (SEL, SEB, SEGR, SHE, etc)
  – Non-Destructive (SEU, SEFI, SET, etc)

• SEE is of major concern for space applications.
  – If not handled well SEE can lead to in worst case catastrophic damage on space crafts.

• Key measures for SEE
  – LET threshold (Energy threshold for protons)
  – Saturation Cross Section
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Bibliography

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